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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/082,441	02/22/2002	L. James Hwang	X-1000 US	6299

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EXAMINER	
WHITMORE, STACY	

ART UNIT	PAPER NUMBER
2825	

DATE MAILED: 09/28/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/082,441	HWANG ET AL.	
	Examiner	Art Unit	
	Stacy A. Whitmore	2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *22 February 2002*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-27* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-27* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *22 February 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *4/29/02,11/24/03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

1. Claims 1-10, 14-23, and 25-27 are rejected under 35 U.S.C. 102(b) as being anticipated by Seidel (US Patent 5,553,001).

As for claim 1, Seidel discloses A method for allocation of resources for a FpGA-based SoC, the method comprising: selecting a first system component for customizing the FpGA-based SoC; determining available resources for the FpGA-based SOC subsequent to said selection of said first system component; and choosing a second system component to utilize said available resources to facilitate allocation of FpGA-based Soc resources [abstract, col. 3, lines 1-15, 32-35, and 60-62, also col. 5, lines 7-11, col. 6, lines 14-24].

As for claim 2, The method according to claim 1, wherein said determining step further comprises determining total FPGA- based Soc resources [abstract, col. 3, lines 1-15, 32-35, and 60-62].

As for claim 3, The method according to claim 2, wherein said step of determining available resources further comprises computing a difference between said total FpGA-based SOC resources and resources utilized by said selected system component, to yield said determined available resources for the FpGA-based SoC [abstract, col. 3, lines 1-15, 32-35, and 60-62, the itemizing and accounting are forms of computing a difference of resources utilizes by components].

As for claim 4, The method according to claim 3, further comprising the step of choosing a third system component that utilizes no more than said available resources when said second system component utilizes more resources that said determined available resources, said third system component being an alternative said second system component [col. 3, lines 1-15 – any number of user's logic or components can be inserted and wherein the usage of resources is checked and determined if compatible with resources].

As for claim 5, The method according to claim 4, wherein said step of choosing said third system component further comprises computing total resources utilized by said first system component and said third system component [col. 3, lines 1-15 – any number of user's logic or components can be inserted and wherein the usage of resources is checked and determined if compatible with resources, all resources are checked for implementation of user logic].

As for claim 6, The method according to claim 5, wherein said step of choosing said third system component further comprises computing a difference between said determined available resources for the FpGA-based SOC and said computed total resources utilized by said first system component and said third system component [abstract, col. 3, lines 1-15, 32-35, and 60-62, the itemizing and accounting are forms of computing a difference of resources utilizes by components].

As for claim 7, The method according to claim 1, further comprises displaying each of said determined available resources for the FpGA-based SoC, and each resource utilized by said first and said second system component [col. 3, line 66 – col. 4, line 3].

As for claim 8, The method according to claim 1, wherein said selecting step further comprises selecting a system component from a group consisting of hardware cores, software cores, hardware core parameters and software core parameters, buses, fixed- function FPGA resources, and user-specified design components [col. 3, lines 1-15, also col. 5, lines 7-11, col. 6, lines 14-24].

As for claim 9, A method for allocation of resources for a FpGA-based soc, the method comprising: selecting system components for customizing the FPGA- based

SoC; computing resource usage for said selected system components; and distributing the FpGA-based SOC system resources among said selected system components according to said computed resource usage to customize said FpGA-based SoC [abstract, col. 3, lines 1-15, 32-35, and 60-62, also col. 5, lines 7-11, col. 6, lines 14-24].

As for claim 10, The method according to claim 9, wherein said step of computing said resource usage further comprises determining resources to be used by at least one selected system component and determining FpGA-based SOC resources available for use by at least an unselected system component [abstract, col. 3, lines 1-15, 32-35, and 60-62].

As for claim 11, The method according to claim 10, further comprising: if said selected system component requires more FpGA-based Soc resources than said available FpGA-based SOC resources, providing an unavailable resource notification []. As for claim 12, The method according to claim further comprising the step of determining at least one alternative system component requiring less resources than said available FpGA-based SOC resources [].

As for claim 13, The method according to claim 12, wherein said determining step further comprises selecting said determined at least one alternative system component to customize the FpGA-based SoC [].

As for claim 14, The method according to claim 9, wherein said computing step further comprises determining incompatibility between said selected system components [col. 3, lines 1-15].

As for claim 15, The method according to claim 14, wherein said determining step further comprises determining at least one alternative compatible system component for replacing an incompatible system component [col. 3, lines 1-15, any user's logic may be implemented in order to meet requirements for resources].

As for claim 16, The method according to claim 9, wherein said selecting step further comprises selecting a system component from a group consisting of hardware cores, software cores, hardware core parameters and software core parameters, buses, fixed- function FPGA resources, and user-specified design components [col. 3, lines 1-15, also col. 5, lines 7-11, col. 6, lines 14-24].

As for claim 17, The method according to claim 16, further comprising the step of selecting a default parameter for said selected system component [col. 4, lines 16-45].

As for claim 18, The method according to claim 17, wherein said step of said selected system component further comprises the step of propagating said default parameter throughout said customization of the FPGA- based SoC [col. 4, lines 16-45].

As for claim 19, A machine readable storage having stored thereon, a computer program having a plurality of code sections, said code sections executable by a machine for causing the machine perform the steps of: selecting a first system component for allocating resources while customizing a FpGA-based SoC; determining available resources for said FpGA-based SOC subsequent to said selection of said first system component; and choosing a second system component to utilize said available resources to facilitate allocation of FpGA-based Soc resources [abstract, col. 3, lines 1-15, 32-35, and 60-62, also col. 5, lines 7-11, col. 6, lines 14-24].

As for claim 20, The machine readable storage according to claim 19, wherein said determining step further comprises determining total FpGA-based SOC resources [abstract, col. 3, lines 1-15, 32-35, and 60-62].

As for claim 21, The machine readable storage according to claim 20, wherein said step of determining available resources further comprises computing a difference between said total FPGA- based Soc resources and resources utilized by said selected system component, to yield said determined available resources for the FpGA-based SoC [abstract, col. 3, lines 1-15, 32-35, and 60-62, the itemizing and accounting are forms of computing a difference of resources utilizes by components].

As for claim 22, A machine readable storage having stored thereon, a computer program having a plurality of code sections, said code sections executable by a machine for causing the machine to perform the steps of: selecting system components for allocating resources for customizing a FpGA-based SoC; computing resource usage for said selected system components; and distributing the FpGA-based SOC system resources among said selected system components according to said computed resource usage to customize said FpGA-based SoC [abstract, col. 3, lines 1-15, 32-35, and 60-62, also col. 5, lines 7-11, col. 6, lines 14-24].

As for claim 23, The machine readable storage according to claim 22 wherein said step of computing said resource usage further comprises determining resources to be used by at least one selected system component and determining FpGA-based SOC resources available for use by an unselected system component [abstract, col. 3, lines 1-15, 32-35, and 60-62].

As for claim 25, The machine readable storage according to claim 22, wherein said computing step further comprises determining incompatibility between said selected system components [col. 3, lines 1-15 – incompatibility is determined in order to match user logic to resources].

As for claim 26, The machine readable storage according to claim 25, wherein said determining step further comprising determining at least one alternative compatible system component for replacing an incompatible system component [col. 3, lines 1-15 – any number of user logic may be implemented as replacement to meet resource allocation].

As for claim 27, The machine readable storage according to claim 22, wherein said selecting step further comprises selecting a system component from a group consisting of hardware cores, software cores, hardware core parameters and a software core parameters, buses, fixed-function FPGA resources, and user- specified design components [abstract, col. 3, lines 1-15, 32-35, and 60-62].

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 11-13, and 24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Seidel (US Patent 5,553,001) in view of Fong (US Patent 6,366,945).

As for claims 11-13, and 24, Seidel discloses the invention substantially as claimed, including the method for allocation of resources for a FpGA-based SoC, and machine readable medium comprising a computer program having a plurality of code section for performing the steps as cited above in the rejections of claims 1-10, 14-16, 19-23, and 25-27 above. As for claims 12-13, Seidel further discloses determining at least one alternative system component requiring less resources than said available FpGA-based SOC resources [col. 3, lines 1-15]; selecting said determined at least one alternative system component to customize the FpGA-based SoC [col. 3, lines 1-15]; and

Seidel does not specifically disclose if said selected system component requires more FpGA-based Soc resources than said available FpGA-based SOC resources, providing an unavailable resource notification.

Fong discloses providing an unavailable resource notification [col. 7 – 8, especially col. 8, lines 13-14].

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Seidel and Fong because providing a notification of unavailable resources within Seidel's system would have improved Seidel's system by notifying a designer during the design process that a change needs to be made, thereby preventing erroneous design choices for alternative user logic presented by a designer.

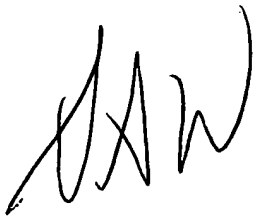
3. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Stacy A. Whitmore whose telephone number is (571)

272-1685. The examiner can normally be reached on Monday-Thursday, alternate Friday 6:30am - 4:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Smith can be reached on (571) 272-1907. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Stacy A Whitmore
Primary Examiner
Art Unit 2825



SAW
September 21, 2005